## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments, see p. 8-11, filed August 14, 2008, with respect to the 35 U.S.C. 103(a) rejections have been fully considered and are persuasive. The 35 U.S.C. 103(a) rejections of Claims 1-22 have been withdrawn.

2. Applicant argues that in Saito (US005774134A), the data from the frame memory 14 (external memory) is not passed to the frame memory 19 (internal memory) and to the display control unit 24 during the same time period (p. 9). There is no suggestion in either Saito or Yoshikawa (US006393520B2) to replace the frame memory 19 or the transfer area 22 of Saito with the external memory 48 of Yoshikawa (p. 10).

In reply, the Examiner agrees that since Saito already teaches an external memory (frame memory 14), there would be no motivation to replace the transfer area 22 of Saito with the external memory 48 of Yoshikawa. Therefore, the Examiner agrees that the combination of references do not teach all of the claimed limitations, and the rejections have been withdrawn.

### *Allowable Subject Matter*

3. Claims 1-22 are allowed.

The following is an examiner's statement of reasons for allowance:

4. The prior art taken singly or in combination do not teach or suggest the combination of all of the limitations of independent Claims 1, 9, and 16. Claims 2-8, 10-15, and 17-22 depend from these independent claims, and therefore also contain allowable subject matter.

5. The closest prior art (Saito US005774134A) teaches apparatus comprising display control unit (24, Fig. 7); display area 23 coupled to display control unit 24 (c. 5, ll. 42-55; c. 6, ll. 4-8).

When storing image data of one frame is completed, image data is transferred from transfer area 22 to display area 23, and, also, is directly provided for image output unit (20) (c. 5, ll. 49-52), which comprises display control unit 24 (c. 5, ll. 56-60). As shown in Fig. 7, data is transferred from transfer area 22 to display area 23, and, also, is directly provided for display control unit 24 (c. 5, ll. 49-60). Fig. 7 shows control circuitry (28) controls these transferring operations (c. 5, ll. 67-c. 6, ll. 4). So, Saito teaches control circuitry (28, Fig. 7) to copy display data from transfer area 22 to display area 23 during reading of same display data by display control unit 24 from transfer area 22 (c. 5, ll. 49-60; c. 5, ll. 67-c. 6, ll. 4). However, Saito does not teach that the data from the frame memory 14 (external memory) is passed to the frame memory 19 (internal memory) and to the display control unit 24 during the same time period.

6. Another prior art (Yoshikawa US006393520B2) teaches apparatus comprising processing unit (13, Fig. 6) that decides which of frame buffers is being read or written (c. 9, ll. 16-18), and D/A converter (19) outputs video data to monitor from frame buffers (c. 9, ll. 25-28). So, processing unit and D/A converter are considered to be display controller. Yoshikawa teaches internal frame buffer (12) coupled to display controller (c. 9, ll. 6-8; c. 9, ll. 25-28); and control circuitry (15) to copy display data from external frame buffer (14) to internal frame buffer, wherein display data copied into internal frame buffer is same display data read by display controller from external frame buffer (c. 9, ll. 47-56; c. 7, ll. 11-15; c. 9, ll. 29-31, 58-67). However, Yoshikawa does not teach copying display data from an external frame buffer to the internal frame buffer during reading of the same display data by the display controller from the external frame buffer.

7. Another prior art (Takala US006909434B2) teaches after display data is copied from external frame buffer (12, Fig. 1) to internal frame buffer (22), internal frame buffer is only updated after new frame is available in external frame buffer (c. 2, ll. 1-19). However, Takala does not teach copying display data from an external frame buffer to the internal frame buffer during reading of the same display data by the display controller from the external frame buffer.

8. Another prior art (Pope US005847705A) teaches display data is transferred from second frame buffer (18) to first frame buffer (20), and copy of display data remains in second frame buffer after it has been transferred (c. 7, ll. 36-49). So, Pope teaches same display data is located in first frame buffer (20) and second frame buffer (18) until new frame buffer is available in second frame buffer (c. 7, ll. 36-49). However, Pope does not teach copying display data from an external frame buffer to the internal frame buffer during reading of the same display data by the display controller from the external frame buffer.

9. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONI HSU whose telephone number is (571)272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kee M Tung/
Supervisory Patent Examiner, Art Unit 2628

JH